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Jameco Part Number 51692

OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM80C48/49/50
MSM80C35/39/40

CMOS 8-Bit Microcontroller

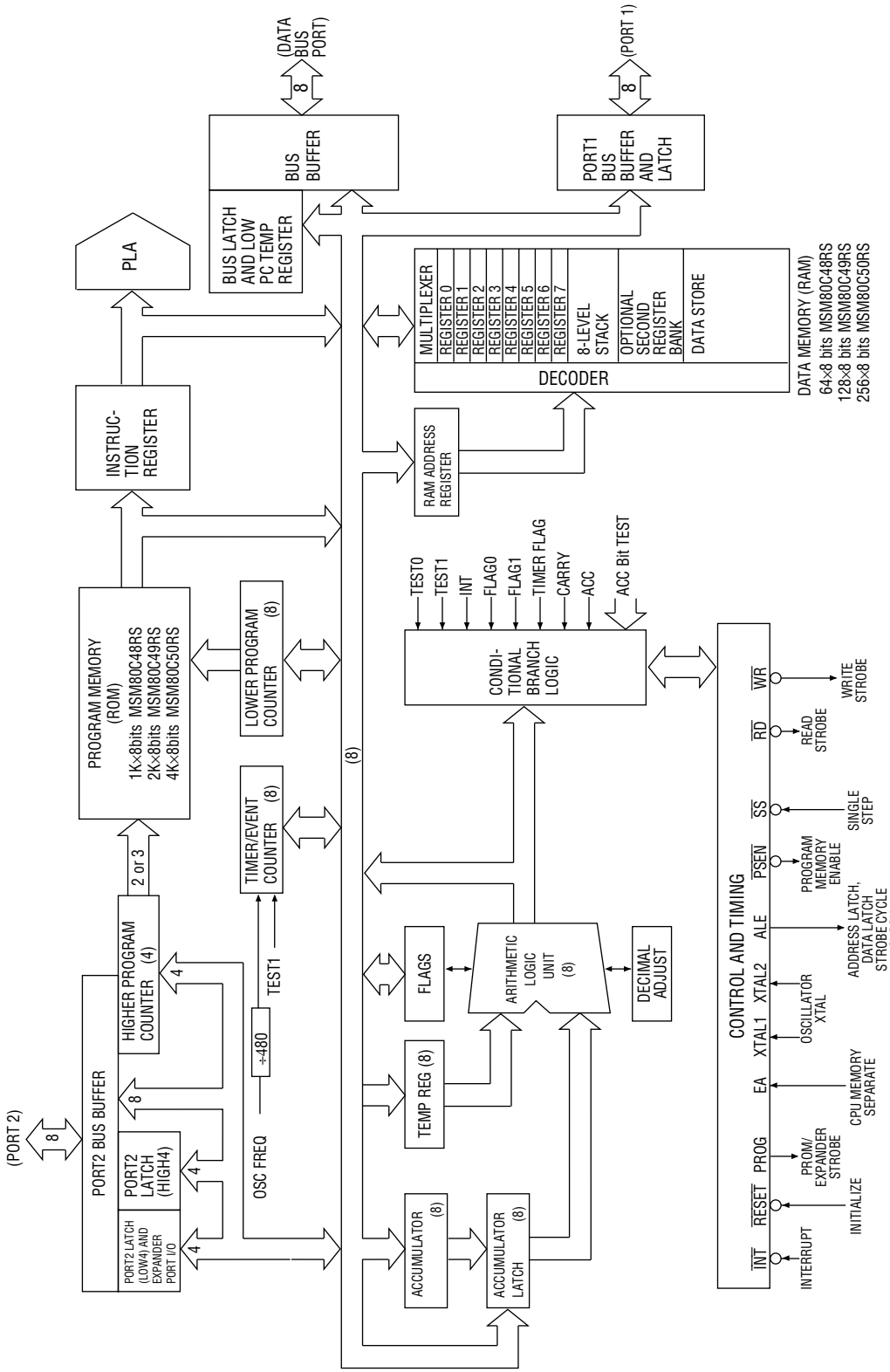
GENERAL DESCRIPTION

The OKI MSM80C48/MSM80C49/MSM80C50 are 8-bit, low-power, high-performance microcontrollers implemented in silicon-gate complementary metal-oxide semiconductor technology. Integrated within these chips are 8K/16K/32K bits of mask program ROM, 512/1024/2048 bits of data RAM, 27 I/O lines, built-in 8 bit timer/counter, and oscillator. Program memory and data paths are byte wide. Eleven new instructions have been added to the NMOS version's instruction set, thereby optimizing power down, port data transfer, decrement and port float functions. Available in 40-pin plastic DIP (RS) or 44-pin plastic flat packages QFP (GSK).

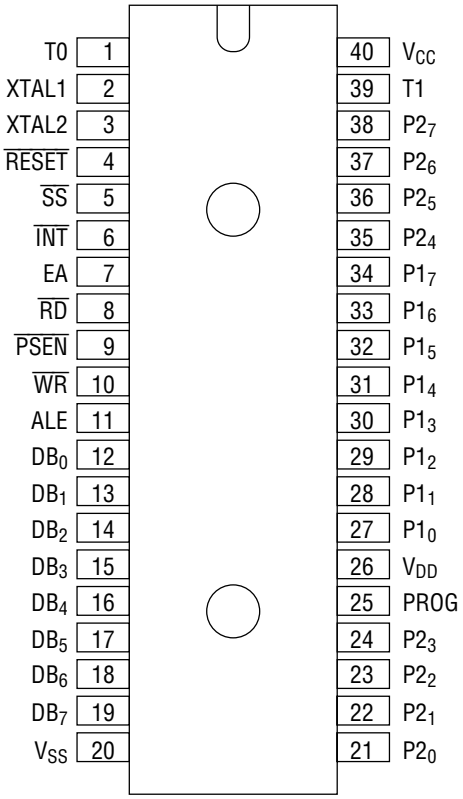
FEATURES

- Lower power consumption enabled by CMOS silicon gate process
- Completely static operation
- Improved power-down feature
- Instruction cycle : 1.36 µs (11 MHz) V_{CC}=4.5 to 6.0 V (MSM80C48/49)
  2.5 µs (6 MHz) V_{CC}=3.5 to 6.0 V (MSM80C50)
- 111 instructions
- All instructions are usable even during execution of external ROM instructions.
- Operation facility
  Addition, logical operations, and decimal adjust
- Program memory (ROM) : 1K words × 8 bits (MSM80C48)
  : 2K words × 8 bits (MSM80C49)
  : 4K words × 8 bits (MSM80C50)
- Data memory (RAM) : 64 words × 8 bits (MSM80C48)
  : 128 words × 8 bits (MSM80C49)
  : 256 words × 8 bits (MSM80C50)
- Two sets of working registers
- External and timer interrupts
- Two test inputs
- Built-in 8-bit timer counter
- Extendable external memory and I/O ports
- I/O port
  Input-output port : 2 ports × 8 bits
  Data bus input-output port : 1 port × 8 bits
- Single-step execution function
- Wide range of operating voltage, from + 2.5 V to + 6 V of V_{CC}
- High noise margin action
- Compatible with Intel's 8048, 8049 and 8050
- Package
  40-pin plastic DIP (DIP40-P-600-2.54) : (MSM80C48-×××RS)
  (MSM80C49-×××RS)
  (MSM80C50-×××RS)
  (MSM80C35RS)
  (MSM80C39RS)
  (MSM80C40RS)
  44-pin plastic QFP(QFP44-P-910-0.80-2K) : (MSM80C48-×××GS-2K)
  (MSM80C49-×××GS-2K)
  (MSM80C50-×××GS-2K)
  (MSM80C35GS-2K)
  (MSM80C39GS-2K)
  (MSM80C40GS-2K)
  ××× indicates the code number.

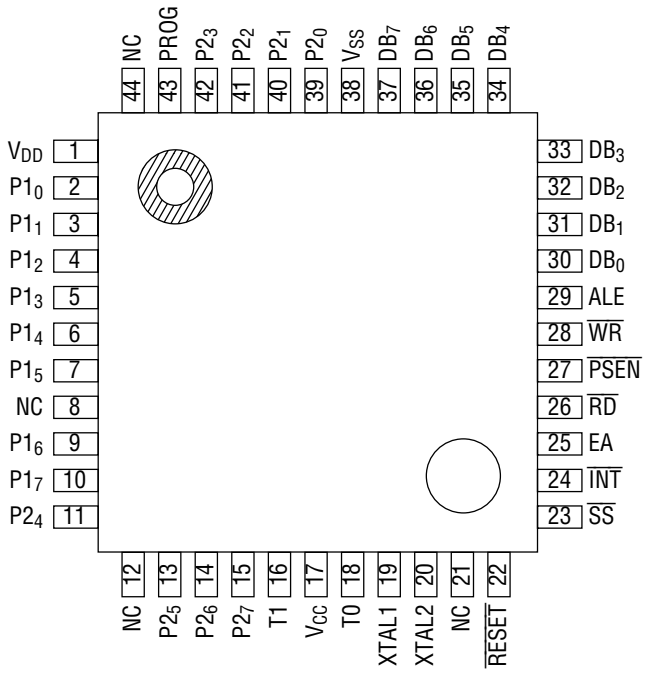
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



40-Pin Plastic DIP



NC: No-connection pin

44-Pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description
$P1_0$-$P1_7$ (PORT 1)	I/O	8-bit quasi-bidirectional port
$P2_0$-$P2_7$ (PORT 2)	I/O	8-bit quasi-bidirectional port The high-order four bits of external program memory addresses can be output from P2.0-P2.3, to which the I/O expander MSM82C43RS may also be connected.
DB_0-DB_7 (BUS)	I/O	Bidirectional port The low-order eight bits of external program memory address can be output from this port, and the addressed instruction is fetched under the control of $\overline{PSEN}$ signal. Also, the external data memory address is output, and data is read and written synchronously using $\overline{RD}$ and $\overline{WR}$ signals. The port can also serve as either a statically latched output port or a non-latching input port.
T0 (Test 0)	I/O	The input can be tested with the conditional jump instructions JT0 and JNT0. The execution of the ENT0 CLK instruction causes a clock output.
T1 (Test 1)	I	The input can be tested with the conditional jump instructions JT1 and JNT1. The execution of a STRT CNT instruction causes an internal counter input.
$\overline{INT}$ (Interrupt)	I	Interrupt input. If interrupt is enabled, $\overline{INT}$ input initiates an interrupt. Interrupt is disabled after a reset. Also testable with a JNI instruction. Can be used to terminate the power-down mode. (Active "0" level)
$\overline{RD}$ (Read)	O	A signal to read data from external data memory. (Active "0" level)
$\overline{WR}$ (Write)	O	A signal to write data to external data memory. (Active "0" level)
ALE Address & Data Latch Clock	O	This signal is generated in each cycle. It may be used as a clock output. External data memory or external program memory is addressed upon the falling edge. For the external ROM, this signal is used to latch the bus port data upon the ALE signal rise-up after the execution of the OUTL BUS, A instruction.
$\overline{PSEN}$ Program Store Enable	O	A signal to fetch an instruction from external program memory (Active "0" level)
$\overline{RESET}$	I	$\overline{RESET}$ input initialize the processor. (Active "0" level) Used to terminate the power-down mode.
$\overline{SS}$ (Single Step)	I	A program is executed step by step. This pin can also be used to control internal oscillation when the power-down mode is reset. (Active "0" level)
EA (External Access)	I	When held at high level, all instructions are fetched from external memory. (Active "1" level)
$\overline{PROG}$ (Expander Strobe)	O	This output strobes the MSM82C43RS I/O expander.

PIN DESCRIPTIONS (Continued)

Symbol	Type	Description
XTAL1 (Crystal 1)	I	One side of the internal crystal oscillator. An external clock can also be input.
XTAL2 (Crystal 2)	O	Other side of the internal crystal oscillator.
V_{CC}	—	Power supply pin
V_{DD}	—	Standby control input. Normally, "1" level. When set to "0" level, oscillation is stopped and prosessor goes into standby mode.
V_{SS}	—	GND

Note: A minimum of two machine cycles are required in $\overline{\text{RESET}}$ pulse duration under the specified power supply and stable oscillator frequency.

ABSOLUTE MAXIMUM RATINGS

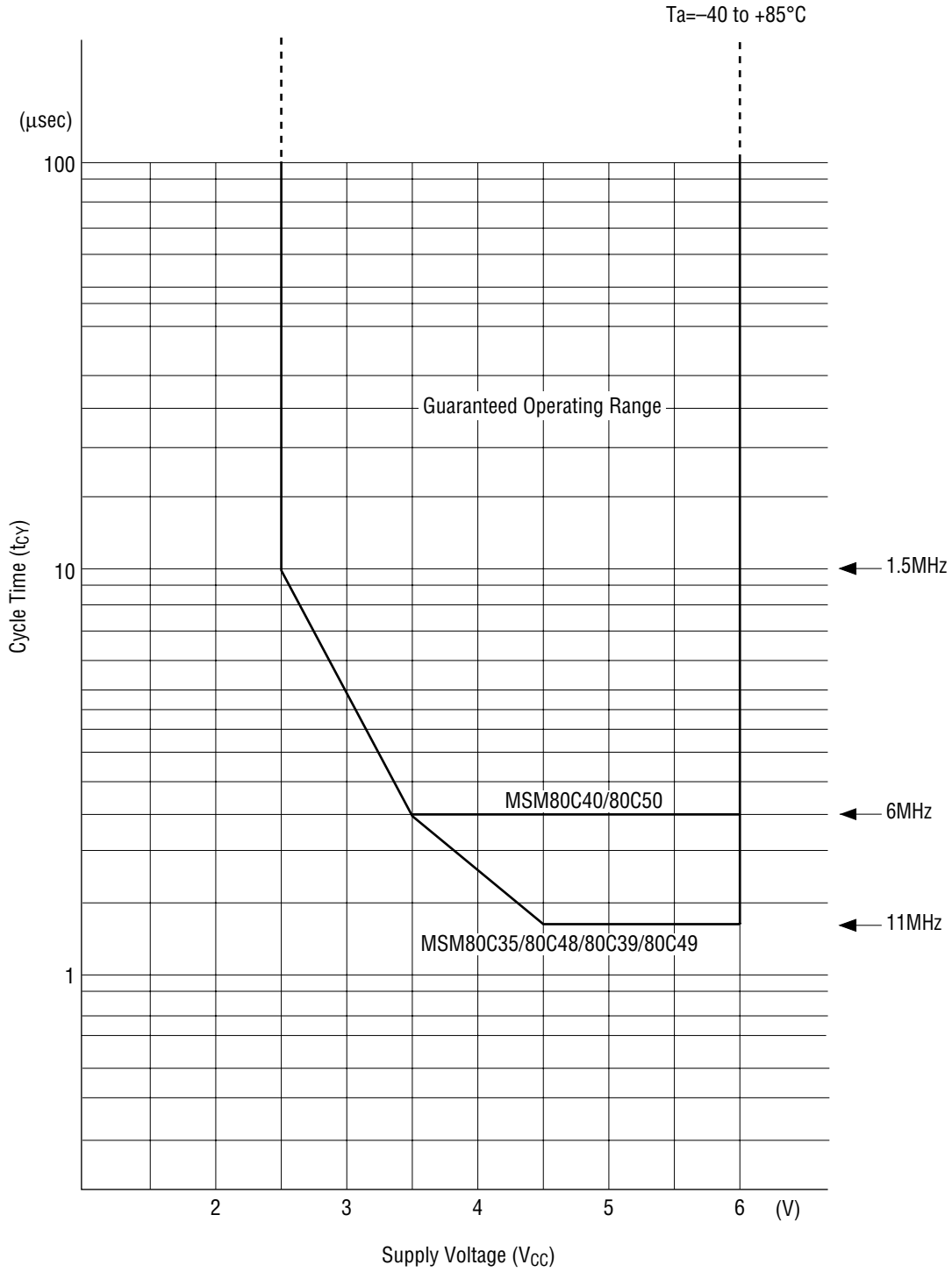
Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{CC}	Ta=25°C	–0.5 to 7	V
Input Voltage	V_I	Ta=25°C	–0.3 to V_{CC} +0.5	V
Storage Temperature	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{CC}	f_{OSC}=DC to 11MHz*	+2.5 to +6	V
Ambient Temperature	T_a	—	–40 to +85	°C
Fan Out	N	MOS load	10	—
		TTL load	1	—

* Minimum operating voltage is dependent on frequency.

MSM80C48/49/50 guaranteed operating range



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC}=5 V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
"L" Input Voltage	V_{IL}	—	–0.5	—	0.13 V_{CC}	V	1
"H" Input Voltage *1	V_{IH}	—	0.4 V_{CC}	—	V_{CC}	V	
"H" Input Voltage *2	V_{IH}	—	0.7 V_{CC}	—	V_{CC}	V	
"L" Output Voltage *3	V_{OL}	I_{OL}=2 mA	—	—	0.45	V	
"L" Output Voltage *4	V_{OL}	I_{OL}=1.6 mA	—	—	0.45	V	
"H" Output Voltage *3	V_{OH}	I_{OH}=–400 µA	0.75 V_{CC}	—	—	V	
"H" Output Voltage *4	V_{OH}	I_{OH}=–50 µA	0.75 V_{CC}	—	—	V	
"H" Output Voltage *3	V_{OH}	I_{OH}=–20 µA	0.93 V_{CC}	—	—	V	
"H" Output Voltage *4	V_{OH}	I_{OH}=–10 µA	0.93 V_{CC}	—	—	V	
Input Leakage Curent	I_{IL}	$V_{SS} \le V_{IN} \le V_{CC}$	—	—	±5	µA	2
Output Leakage Current *5	I_{OL}	$V_{SS} \le V_O \le V_{CC}$	—	—	±5	µA	3
$\overline{\text{RESET}}$ Input current	I_R	V_{IN}=0.7 V_{CC}	–20	–50	–80	µA	2
		V_{IN}=0.13 V_{CC}	–3	–8	–15	µA	
$\overline{\text{SS}}$ Input current *6	I_{SS}	Pull-up (V_{IN}=V_{IL})	20	50	80	µA	
		Pull-down (V_{IN}=V_{IH})	–6	–15	–25	µA	
P1, P2 input current	I_{P1}, I_{P2}	V_{IN}=V_{IH}	–300	–600	–900	µA	2
		V_{IN}=V_{IL}	–10	–40	–80	µA	
Power Down Mode Standby Current	I_{CCS}	At hardware power down *7 Ta=25°C, V_{CC}=2.0 V	—	—	10	µA	4
		At HLTS execution *7 Ta=25°C, V_{CC}=2.0 V	—	—	10		
Power Supply Current (Halt Mode)	I_{CC}	V_{CC}=4 V, f=1 MHz	—	—	0.5	mA	
		V_{CC}=4 V, f=6 MHz	—	—	1.0		
		V_{CC}=4 V, f=11 MHz	—	—	2.0		
		V_{CC}=5 V, f=1 MHz	—	—	1.0		
		V_{CC}=5 V, f=6 MHz	—	—	2.0		
		V_{CC}=5 V, f=11 MHz	—	—	3.0		
		V_{CC}=6 V, f=1 MHz	—	—	1.5		
		V_{CC}=6 V, f=6 MHz	—	—	3.0		
		V_{CC}=6 V, f=11 MHz	—	—	5.0		
Power Supply Current	I_{CC}	V_{CC}=4 V, f=1 MHz	—	—	1.5	mA	
		V_{CC}=4 V, f=6 MHz	—	—	5.0		
		V_{CC}=4 V, f=11 MHz	—	—	10		
		V_{CC}=5 V, f=1 MHz	—	—	2.5		
		V_{CC}=5 V, f=6 MHz	—	—	7.5		
		V_{CC}=5 V, f=11 MHz	—	—	15		
		V_{CC}=6 V, f=1 MHz	—	—	5.0		
		V_{CC}=6 V, f=6 MHz	—	—	10		
		V_{CC}=6 V, f=11 MHz	—	—	20		

*1 This does not apply to RESET, XTAL1, XTAL2, V_{DD}, and EA.
*2 RESET, XTAL1, XTAL2, V_{DD}, and EA.
*3 BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG
*4 Other outputs
*5 High-impedance state
*6 This operates as a pull-down resistor when the oscillation is stopped in the HLTS or V_{DD} power-down mode and as a pull-up resistor in other states.
*7 This does not contain flow out current from I/O ports and signal pins.

AC Characteristics

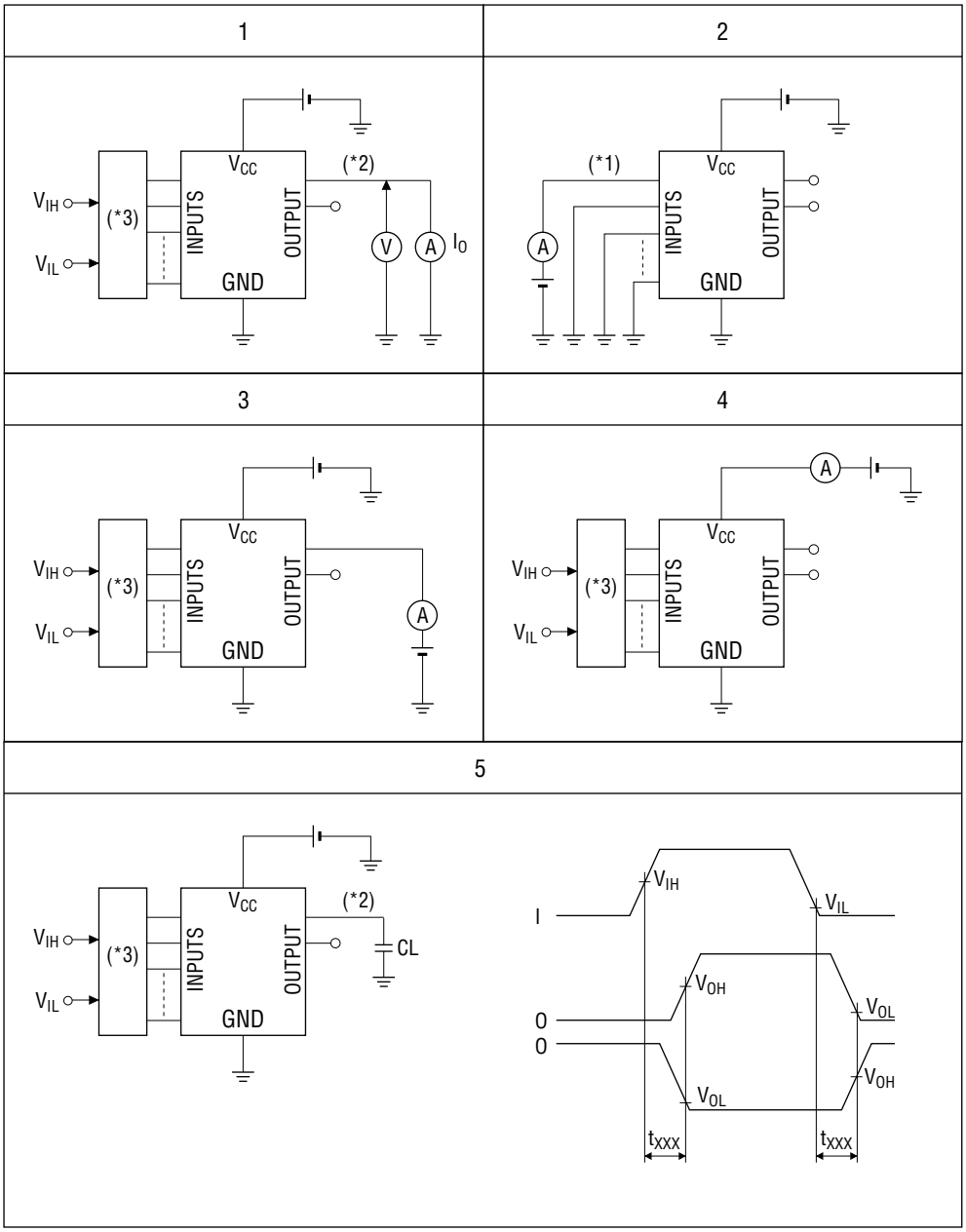
(V_{CC}=2.5V to 6V (*1), Ta=–40 to +85°C)

Parameter	Symbol	V_{CC}=5 V±10% 11 MHz Clock		Variable clock 0 to 11 MHz		Unit
		Min.	Max.	Min.	Max.	
ALE Pulse Width	t_{LL}	150	—	3.5t–170	—	ns
Address Setup Time (up to ALE)	t_{AL}	70	—	2t–110	—	ns
Address Hold Time (from ALE)	t_{LA}	50	—	t–40	—	ns
Bus Port Latch Data Setup Time (up to ALE Rising Edge)	t_{BL}	110	—	2.5t –115	—	ns
Bus Port Latch Data Hold Time (from ALE Rising Edge)	t_{LB}	90	—	1.5 t–45	—	ns
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	480	—	7t–155	—	ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	350	—	6t–200	—	ns
Data Setup Time (before $\overline{WR}$)	t_{DW}	390	—	6t–155	—	ns
Data Hold after Time (after $\overline{WR}$)	t_{WD}	40	—	2t–140	—	ns
Data Hold Time (after $\overline{RD}$, $\overline{PSEN}$)	t_{DR}	0	110	0	1.5t–30	ns
$\overline{RD}$ to Data-in	t_{RD1}	—	350	—	5t–265	ns
$\overline{PSEN}$ to Data-in	t_{RD2}	—	190	—	5t–265	ns
Address Setup to $\overline{WR}$	t_{AW}	300	—	6t–245	—	ns
Address Setup to Data-in	t_{AD1}	—	730	—	12t–360	ns
Address Setup to Instruction	t_{AD2}	—	460	—	8t–265	ns
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	140	—	2t–40	—	ns
Address Float to $\overline{PSEN}$	t_{AFC2}	10	—	10	—	ns
Control Pulse Setup Time from ALE ($\overline{PSEN}$)	t_{LAFC2}	60	—	t–30	—	ns
Control Pulse Setup Time from ALE ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	200	—	3t–75	—	ns
Control Pulse up to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	50	—	1.5t–85	—	ns
Control Pulse up to ALE ($\overline{PSEN}$)	t_{CA2}	320	—	4.5t–90	—	ns
Port Control Setup Time (up to PROG Falling Edge)	t_{CP}	50	—	2t–130	—	ns
Port Control Hold Time (from PROG Falling Edge)	t_{PC}	100	—	4t–260	—	ns
$\overline{PROG}$ to Input Data Valid	t_{PR}	—	650	—	9t–170	ns
Input Data Hold Time	t_{PF}	0	140	0	1.5t	ns
Output Data Setup Time	t_{DP}	250	—	6t–290	—	ns
Output Data Hold Time	t_{PD}	40	—	3t–230	—	ns
$\overline{PROG}$ Pulse Width	t_{PP}	700	—	10t–210	—	ns
Port 2 I/O Setup Time	t_{PL}	160	—	4.5–250	—	ns
Port 2 I/O Hold Time	t_{LP}	15	—	1.5t–120	—	ns
Port Output Data (from ALE)	t_{PV}	—	510	—	4t+145	ns
T0 Cycle	t_{OPRR}	270	—	3t	—	ns
Instruction Execution Time	t_{CY}	1.36	—	15t	—	µs

Note : Control output : C_L=80pF
Bus output : C_L=150pF [for 20 pF (t_{AL}, t_{AFC1}, t_{AFC2})]

*1 Minimum operating voltage is dependent on frequency.

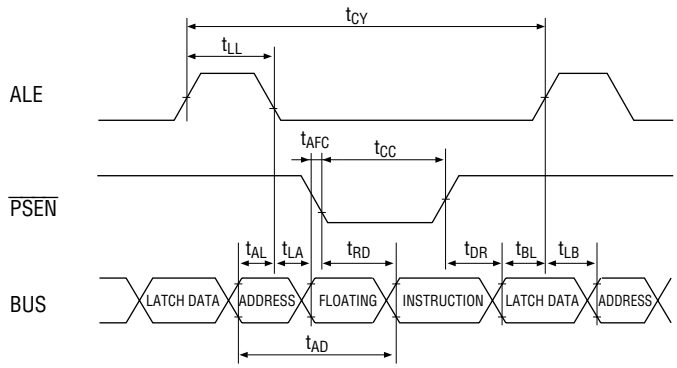
Measuring circuits



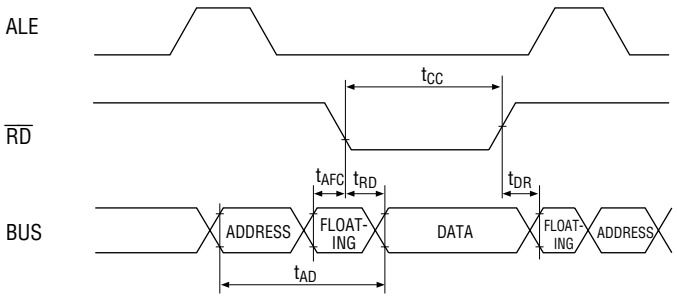
*1 This is repeated for each specified input pin.
*2 This is repeated for each specified output pin.
*3 Input logic for setting the specified state

Timing Diagram

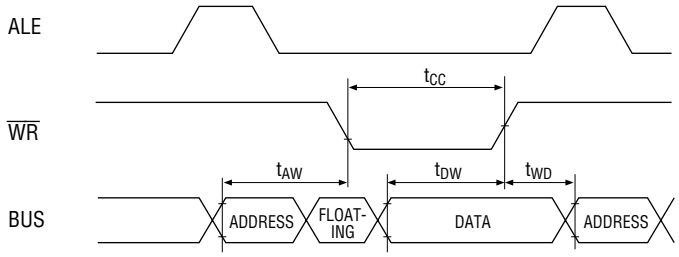
Instruction fetch (from external program memory)



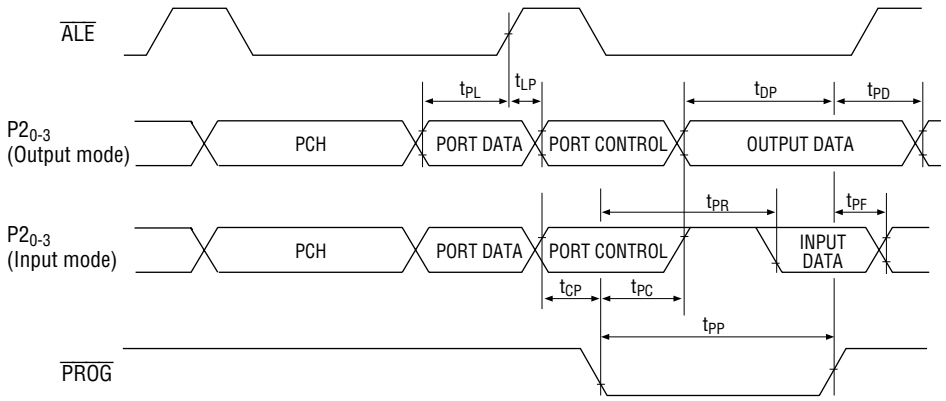
Read (from external data memory)



Write (to external memory)



Low-order 4 bits input/output of port 2 when expanded I/O port is used (in external program memory access mode)



FUNCTIONAL DESCRIPTION

Added Functions of MSM80C48, MSM80C49 and MSM80C50

The MSM80C48, MSM80C49 and MSM80C50 are basically incorporated with the capabilities of Intel's 8048, 8049, and 8050 plus the following new functions:

1. Power-Down Mode Enhancements

1.1 Power-down by software

(1) Clock (See item 4, "Power-down mode", for details.)
   a. Crystal oscillator halt (HLTS instruction)
      Power requirements can be minimized.
   b. Clock supply halt (HALT instruction)
      Restart is accomplished without oscillator wait.

(2) I/O ports
   I/O port floating instructions
   Power consumption resulting from inputs/outputs can be minimized with FLT and FLTT instructions.
   Port floating is cancelled by executing FRES instruction, "0" level at $\overline{INT}$ pin or "0" level at $\overline{RESET}$ pin.

(3) Six types of power-down can be done by a combination of HLTS/HALT and FLT/FLTT instructions.

1.2 Power-down by hardware (See 4.3, Power-down mode by V_{DD} pin utilization for details.)

Crystal oscillators can be halted by controlling the V_{DD} pin, thereby floating all I/O ports for minimum power consumption.

2. Additional Instructions (11)

HLTS	MOV A, P2
HALT	MOVP1, @ R3
FLT	MOVP1 P, @R3
FLTT	DEC @Rr
FRES	DJNZ @ Rr, addr
MOV A, P1	

3. Improved Uses of BUS P_{0-7}, $P1_{0-7}$, $P2_{0-7}$, and $\overline{SS}$ pins

3.1 BUS P_{0-7}

The MSM80C48, MSM80C49, and MSM80C50 remove the limitation on the use of OUTL BUS, A instructions during the external ROM access mode by having an independent data latch and external ROM mode address latch in BUS P_{0-7}.
Consequently, there is no need to relocate bus port instructions when in the external ROM access mode.

3.2 P_{10-7} and $P2_{0-7}$

The MSM80C48, MSM80C49 and MSM 80C50 are designed to minimize power consumption when $P1_{0-7}$ and $P2_{0-7}$ are used as input/output ports, to maximize the performance of CMOS.
When these ports are used as output ports, the acceleration circuit is actuated only when

output data changes from "0" to "1", thus speeding up the rise time of the output signals. When these ports are used as input ports, the internal pull-up resistor becomes approximately 9 kΩ when input data is "1".
The internal pull-up resistor rises to approximately 100 kΩ when input data is "0".
Thus, a high noise margin can be obtained by selecting the impedance and thus the outflow of current is minimized whenever these ports are used as output or input ports.

3.3 Clock generation control via the $\overline{SS}$ pin

When the crystal oscillator is halted in the HLTS or hardware power-down mode, the $\overline{SS}$ pin is pulled down by a resistor of 20 to 50 kΩ, while its internal pull-up resistor of 200 to 500kΩ is isolated from V_{CC}. When the power-down mode is cancelled, the internal resistor of the $\overline{SS}$ pin is changed from pull-down to pull-up. Consequently, the CPU can be halted for any period of time until the crystal oscillator resumes normal oscillation when a capacitor is connected to the $\overline{SS}$ pin.

4. Power-Down Mode

The MSM80C48, MSM80C49, and MSM80C50 power-down mode can be enabled in two different ways through software by a combination of clock control and port floating instructions, and through hardware by control of the V_{DD} pin.

4.1 Software power-down mode

Power-down mode can be done by a combination of the following instructions.

(1) HALT (clock supply halt to control circuit)

Instruction code : | 0 0 0 0 0 0 0 1 |

Description : Although crystal oscillator operation is continued, the clock supply to the CPU control circuit is halted and CPU operations are suspended. When cancelling this software mode, restart is accomplished without oscillator wait.

(2) HLTS (oscillation stop)

Instruction code : | 1 0 0 0 0 0 1 0 |

Description : The oscillator operation is halted and CPU operations are suspended. In cancelling this power down mode, connecting a capacitor to the $\overline{SS}$ pin enables a reasonable wait period to be accomplished before normal operation is resumed. [Except in the case of using the $\overline{RESET}$ pin]

(3) FLT (floating $P1_{0\text{-}7}$, $P2_{0\text{-}7}$, and $BP_{0\text{-}7}$)

Instruction code : | 1 0 1 0 0 0 1 0 |

Description :

	Internal ROM mode	External ROM mode
P1	Floating	Floating
P2	Floating	$P2_{0\text{-}3}$ operation
BP	Floating	Operation

Details of IC pin status as a result of executing the FLT instruction are shown in the above table.

(4) FLTT (floating of all output pins)

Instruction code :

1	1	0	0	0	0	1	0

Description :

	Internal ROM mode	External ROM mode
ALE	Floating	Operation
$\overline{PSEN}$	Floating	Operation
PROG	Floating	Floating
$\overline{WR}$	Floating	Floating
$\overline{PD}$	Floating	Floating
T0 OUT	Floating	Floating
P1	Floating	Floating
P2	Floating	$P2_{0\text{-}3}$ operation
BP	Floating	Operation
XTAL	Operation	Operation

Details of IC pin status as a result of executing the FLTT instruction are shown in above Table.

Example 1 : Power-down mode accomplished by stopping oscillation.
- ❍ Can be set by execution of HLTS [82H] instruction.

Example 2 : Power-down mode accomplished by stopping the clock supply to the CPU control circuit.
- ❍ Can be set by execution of HALT [01H] instruction.

Example 3 : Power-down mode by floating of $P1_{0\text{-}7}$, $P2_{0\text{-}7}$ and $BP_{0\text{-}7}$, and subsequent stopping of CPU oscillation.
- ❍ Can be set by first executing the FLT [A2H] instruction, followed by the HLTS [82H] instruction.

Example 4 : Power-down mode by floating $P1_{0\text{-}7}$, $P2_{0\text{-}7}$ and $BP_{0\text{-}7}$, and then stopping the clock supply to the CPU control circuit.
- ❍ Can be set by first executing the FLT [A2H] instruction, and then the HALT [01H] instruction.

Example 5 : Power-down mode by floating all output pins, followed by stopping oscillation.
- ❍ Can be set by first executing the FLTT [C2H] instruction followed by execution of the HLTS [82H] instruction.

Example 6 : Power-down mode by floating all output pins, followed by stopping of the clock supply to the CPU control circuit.
- ❍ Can be set by first executing the FLTT [C2H] instruction, followed by execution of the HALT [01H] instruction. Connect the pull-up resistor or pull-down resistor to port pin and fix the output port pin level to either 1or 0 when output port is set to floating.

4.2 Cancellation of software power-down mode

The power-down mode status outlined above in examples 1 to 6 can be cancelled by using either the interrupt pin or the $\overline{\text{RESET}}$ pin.

(1) Use of the $\overline{\text{INT}}$ pin during external interrupt enable mode (i.e. following execution of EN I instruction).

- The clock generator is activated and the CPU is started up when a "0" level is applied to the $\overline{\text{INT}}$ pin. If this "0" level is maintained until the occurrence of at least 2 ALE output signals, an external interrupt is generated, and execution proceeds from address 3. If, however, the power-down is entered during the interrupt processing routine, execution resumes just after the power-down instruction.

(2) Use of the $\overline{\text{INT}}$ pin during external interrupt disable mode (i.e. following execution of DIS I instruction or hardware reset)

- The clock generator is activated and the CPU is started up when a "0" level is applied to the $\overline{\text{INT}}$ pin. When "0" level is maintained until the occurrence of at least 2 ALE output signals, execution is resumed just after the power-down instruction.

(3) Use of the $\overline{\text{RESET}}$ pin

- The clock generator is activated and the CPU started up when a "0" level is applied to the $\overline{\text{RESET}}$ pin. If this "0" level is maintained until the occurrence of at least 2 ALE output signals, the CPU is reset and execution proceeds from address 0. In case cancellation is done in oscillation stop mode, the "0" level must be input to the $\overline{\text{RESET}}$ pin until oscillation is stabilized.

4.3 Hardware power-down mode

In the MSM80C48, MSM80C49 and MSM80C50, forcing the level at the V_{DD} pin to a "0" during either external ROM or internal ROM mode results in suspension of the oscillator function and subsequent floating (high impedance) of all the I/O pins except the $\overline{\text{RESET}}$, $\overline{\text{SS}}$ and XTAL 1/2 pins. The CPU is thereby stopped while maintaining internal status.

4.4 Cancellation of hardware power-down mode

(1) Use of $\overline{\text{RESET}}$ pin
- The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "0" level is input to the $\overline{\text{RESET}}$ pin. If this "0" level is kept applied to the $\overline{\text{RESET}}$ pin until oscillation become stable, the CPU will be reset and will start executing from address 0.

(2) Use of the $\overline{\text{INT}}$ pin during external interrupt enable status (i.e. following execution of EN I instruction)
- The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "0" level is applied to the $\overline{\text{INT}}$ pin. If this "0" level is maintained until the occurrence of at least 2 ALE output signals, an external interrupt is generated, and execution starts from address 3.
  However, if the power-down mode is started during an interrupt processing routine, execution will be continued on the next instruction after the present instruction.

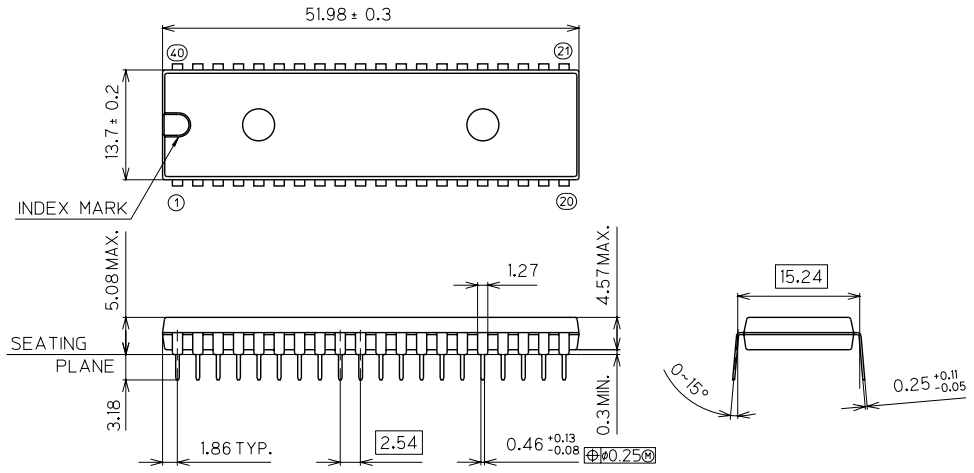
(3) Use of the $\overline{\text{INT}}$ pin during external interrupt disable mode (i.e. following excution of DIS I instruction or hardware reset)
- The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "0" level is applied to the $\overline{\text{INT}}$ pin. If this "0" level is maintained until the occurrence of at least 2 ALE output signals, execution is continued on the next instruction after the present instruction.

(4) Use of V_{DD} pin only
- The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "1" level is also applied to both the $\overline{\text{RESET}}$ and $\overline{\text{INT}}$ pins. In this case, execution is resumed from the stopped position.

PACKAGE DIMENSIONS

(Unit : mm)

DIP40-P-600-2.54



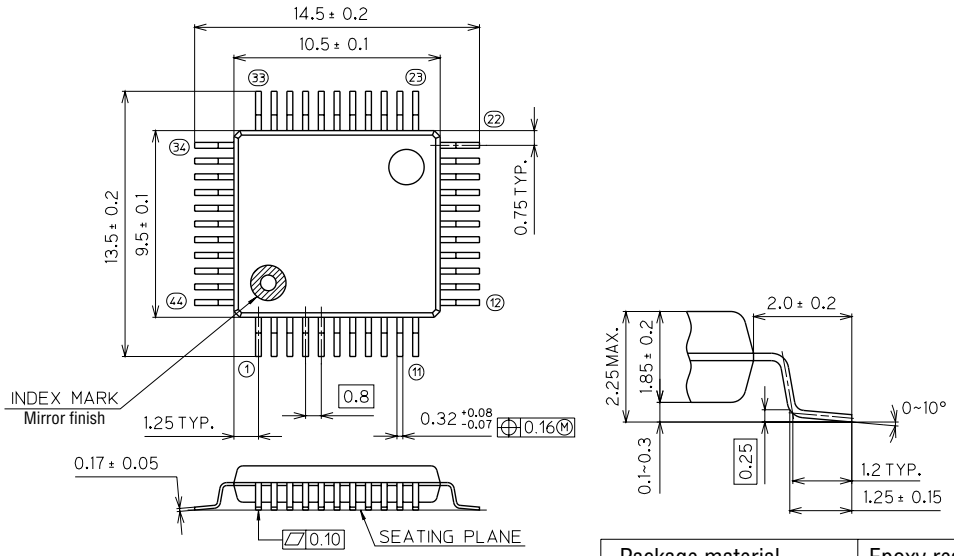
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.10 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).